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1. X **Patent** ***Document No.** ~~JP403077324~~A (JP 03077324 A)
***Country Code** JP
***Publication Date** 04-02-1991
***Language** Japanese
No. of Pages _____ *(filled by STIC)*

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1. 2/34/1 (Item 1 from file: 351)

009467267 **Image available**
WPI Acc No: 1993-160806/199320
Thermal transfer recording sheet - comprises substrate and image-receiving layer comprising transparent receptive layer and white opacifying layer
Patent Assignee: MITSUBISHI CHEM CORP (MITU); MITSUBISHI KASEI CORP (MITU)
Inventor: HIROTA T; KURODA K; SHINOHARA H
Number of Countries: 005 Number of Patents: 006
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
EP 542308	A1	19930519	EP 92119486	A	19921113	199320	B
JP 5139056	A	19930608	JP 91300753	A	19911115	199327	
US 5314862	A	19940524	US 92974896	A	19921112	199420	
EP 542308	B1	19950517	EP 92119486	A	19921113	199524	
DE 69202548	E	19950622	DE 602548	A	19921113	199530	
			EP 92119486	A	19921113		
JP 3077324	B2	20000814	JP 91300753	A	19911115	200043	

Priority Applications (No Type Date): JP 91300753 A 19911115
Cited Patents: No-SR.Pub; 1.Jnl.Ref; EP 257633; EP 333873
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
EP 542308	A1	E	11	B41M-005/38	
Designated States (Regional): DE FR GB					
JP 5139056	A		6	B41M-005/38	
US 5314862	A		7	B41M-005/035	
EP 542308	B1	E	13	B41M-005/38	
Designated States (Regional): DE FR GB					
DE 69202548	E			B41M-005/38	Based on patent EP 542308
JP 3077324	B2		6	B41M-005/38	Previous Publ. patent JP 5139056

Abstract (Basic): EP 542308 A

A thermal transfer recording sheet comprises a substrate with an image-receiving layer formed on it, which is thermally transferable onto a record sheet. The image-receiving layer comprises a transparent receptive layer and a white opacifying layer laminated in this order on the substrate, and the opacifying layer contains a plasticiser.

The plasticiser is a cpd. selected from phthalic acid esters, dibasic acid esters, fatty acid esters and epoxy cpds. The white opacifying layer comprises 1 pt. wt. of a white pigment (pref. titanium oxide), 0.5-5 pts. wt. of a binder resin (pref. vinyl-chloride-vinyl acetate copolymer resin or acrylic resin) and 0.05-2.5 pts. wt. of a plasticiser.

USE/ADVANTAGE - An ordinary sheet of paper can be used as a record sheet. The sheet is capable of transferring a clear image simply and with excellent colour reproducibility on a wide range of various types of ordinary sheets of paper. Sharp edges are provided between the heated portion and the non-heated portion at the time of thermal transfer of the image-receiving layer. The image- receiving layer has

excellent adhesiveness with a wide variety of ordinary sheets of paperry
Dwg.1/2

Abstract (Equivalent): EP 542308 B
A thermal transfer recording sheet comprising a substrate (1) and an image-receiving layer (4) formed thereon, which comprises a transparent receptive layer (2) and a white opacifying layer (3) laminated in this order on the substrate (1), and said white opacifying layer (3) is thermally transferable onto a recording sheet together with the transparent receptive layer (2), characterised in that said opacifying layer (2) comprising relative to one part by weight of a white pigment from 0.1 to 20 parts by weight of a binder resin and from 0.01 to 10 parts by weight of a plasticiser.
Dwg.1/2

Abstract (Equivalent): US 5314862 A
Thermal transfer recording sheet comprises a substrate having on it an image receiving layer which is thermally transferable onto a record sheet. The image receiving layer comprises a transparent receiving layer and a white opacifying layer laminated on the substrate. The opacifying layer comprises 1 pt. wt. white pigment, 0.1-20 pts. wt. binder resin and 0.01-10 pts. wt. plasticiser.
Pref., the plasticiser comprises phthalic acid esters, diabasic acid esters, fatty acid esters or epoxy cpds. The opacifying layer contains Ti oxide as white pigment and a vinyl chloride vinyl acetate copolymer resin or an acrylic resin as binder resin. The image receiving layer has a prime coating layer contg. releasing agent between the substrate and transparent receiving layer.
USE/ADVANTAGE - Used for simply transferring clear images with good colour reproducibility. The image receiving layer has good adhesiveness with ordinary sheets of paper.
Dwg.1/2

Derwent Class: A14; A89; E19; G05; P75; T04
International Patent Class (Main): B41M-005/035; B41M-005/38
International Patent Class (Additional): B41M-005/00

☐ 2. 2/34/2 (Item 2 from file: 351)

008634257 **Image available**
WPI Acc No: 1991-138287/ 199119
Semiconductor IC device - has wiring layout in which multilayer wirings are arranged in parallel NoAbstract Dwg 1/7

Patent Assignee: MITSUBISHI DENKI KK (MITQ)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
JP 3077324	A	19910402	JP 89213643	A	19890819	199119	B

Priority Applications (No Type Date): JP 89213643 A 19890819
Derwent Class: U11
International Patent Class (Additional): H01L-021/32

☐ 3.

2/34/3 (Item 3 from file: 347)

03414424 **Image available**

SEMICONDUCTOR INTEGRATED CIRCUIT

Pub. No.: 03-077324 [JP 3077324 A]
Published: April 02, 1991 (19910402)
Inventor: SHINOHARA HIROSHI
KISHI YOSHIYUKI
Applicant: MITSUBISHI ELECTRIC CORP [000601] (A Japanese Company or Corporation), JP (Japan)
Application No.: 01-213643 [JP 89213643]
Filed: August 19, 1989 (19890819)
International Class: [5] H01L-021/3205
JAPIO Class: 42.2 (ELECTRONICS -- Solid State Components)
Journal: Section: E, Section No. 1081, Vol. 15, No. 246, Pg. 51, June 24, 1991 (19910624)

ABSTRACT

PURPOSE: To increase resistance to electromigration, to make wiring region small and to realize a high integration by a method wherein a semiconductor integrated circuit is provided with a plurality of metal wirings layers and a plurality of wiring lines and the metal wiring are piled up in parallel on the same wiring lines over a plurality of layers and connected to each other via through-holes.

CONSTITUTION: Al metal wiring such as power-supply lines 7a, 8a, signal conductors 7b, 8b, grounding conductors 7c, 8c, and the like are piled up in parallel on the same wirings lines over two layers in a semiconductor integrated circuit substrate which is provided with a plurality of metal wiring layers and a plurality of wiring lines; they are connected to each other via through-holes 6. Widths of the Al wirings 7a, 7b, 7c, 8a, 8b, 8c are narrow as compared with those of conventional metal wirings. The widths of the metal wirings are not made wider but are composed of a plurality of layers. Thereby, an electric current is distributed and a current density is suppressed. Since the widths of the wirings are narrow, the area of the semiconductor integrated circuit becomes small, compared with that of conventional circuits.

☐ 4.

2/34/4 (Item 4 from file: 345)

11162335
Basic Patent (No,Kind,Date): EP 542308 A1 19930519

PATENT FAMILY:
GERMANY (DE)
Patent (No,Kind,Date): DE 69202548 C0 19950622
WAERMEEMPFINDLICHE UEBERTRAGUNGSAUFZEICHNUNGSSCHICHT. (German)
Patent Assignee: MITSUBISHI CHEMICAL CORP (JP)
Author (Inventor): HIROTA TAKAO (JP); SHINOHARA HIDEO (JP); KURODA KATSUHIKO (JP)
Priority (No,Kind,Date): JP 91300753 A 19911115
Applic (No,Kind,Date): DE 69202548 A 19921113
IPC: * B41M-005/38; B41M-005/00
CA Abstract No: * 119(18)191950T
JAPIO Reference No: * 170524M000114
Language of Document: German
Patent (No,Kind,Date): DE 69202548 T2 19960222
WAERMEEMPFINDLICHE UEBERTRAGUNGSAUFZEICHNUNGSSCHICHT. (German)
Patent Assignee: MITSUBISHI CHEM CORP (JP)
Author (Inventor): HIROTA TAKAO (JP); SHINOHARA HIDEO (JP); KURODA KATSUHIKO (JP)
Priority (No,Kind,Date): JP 91300753 A 19911115
Applic (No,Kind,Date): DE 69202548 A 19921113
IPC: * B41M-005/38; B41M-005/00
CA Abstract No: * 119(18)191950T
JAPIO Reference No: * 170524M000114
Language of Document: German

EUROPEAN PATENT OFFICE (EP)
Patent (No,Kind,Date): EP 542308 A1 19930519
THERMAL TRANSFER RECORDING SHEET (English; French; German)
Patent Assignee: MITSUBISHI CHEM IND (JP)
Author (Inventor): HIROTA TAKAO (JP); SHINOHARA HIDEO (JP); KURODA KATSUHIKO (JP)
Priority (No,Kind,Date): JP 91300753 A 19911115
Applic (No,Kind,Date): EP 92119486 A 19921113
Designated States: (National) DE; FR; GB
IPC: * B41M-005/38; B41M-005/00
CA Abstract No: ; 119(18)191950T
Language of Document: English
Patent (No,Kind,Date): EP 542308 B1 19950517
THERMAL TRANSFER RECORDING SHEET. (English; French; German)
Patent Assignee: MITSUBISHI CHEM CORP (JP)
Author (Inventor): HIROTA TAKAO (JP); SHINOHARA HIDEO (JP); KURODA KATSUHIKO (JP)
Priority (No,Kind,Date): JP 91300753 A 19911115
Applic (No,Kind,Date): EP 92119486 A 19921113
Designated States: (National) DE; FR; GB
IPC: * B41M-005/38; B41M-005/00
CA Abstract No: * 119(18)191950T
JAPIO Reference No: * 170524M000114
Language of Document: English

JAPAN (JP)
Patent (No,Kind,Date): JP 5139056 A2 19930608
SHEET FOR THERMAL TRANSFER RECORDING (English)
Patent Assignee: MITSUBISHI CHEM IND
Author (Inventor): HIROTA TAKAO; SHINOHARA HIDEO; KURODA KATSUHIKO
Priority (No,Kind,Date): JP 91300753 A 19911115

Applic (No,Kind,Date): JP 91300753 A 19911115
IPC: * B41M-005/38
JAPIO Reference No: ; 170524M000114
Language of Document: Japanese
Patent (No,Kind,Date): JP 3077324 B2 20000814
Patent Assignee: MITSUBISHI CHEM CORP
Author (Inventor): HIROTA TAKAO; SHINOHARA HIDEO; KURODA KATSUHIKO
Priority (No,Kind,Date): JP 91300753 A 19911115
Applic (No,Kind,Date): JP 91300753 A 19911115
IPC: * B41M-005/38
Language of Document: Japanese

UNITED STATES OF AMERICA (US)
Patent (No,Kind,Date): US 5314862 A 19940524
THERMAL TRANSFER RECORDING SHEET (English)
Patent Assignee: MITSUBISHI CHEM IND (JP)
Author (Inventor): HIROTA TAKAO (JP); SHINOHARA HIDEO (JP); KURODA KATSUHIKO (JP)
Priority (No,Kind,Date): JP 91300753 A 19911115
Applic (No,Kind,Date): US 974896 A 19921112
National Class: * 503227000; 428195000; 428207000; 428500000; 428522000; 428913000; 428914000
IPC: * B41M-005/035; B41M-005/38
CA Abstract No: * 119(18)191950T
JAPIO Reference No: * 170524M000114
Language of Document: English

☐ 5. 2/34/5 (Item 5 from file: 345)

9816022
Basic Patent (No,Kind,Date): JP 3077324 A2 910402

PATENT FAMILY:
JAPAN (JP)
Patent (No,Kind,Date): JP 3077324 A2 910402
SEMICONDUCTOR INTEGRATED CIRCUIT (English)
Patent Assignee: MITSUBISHI ELECTRIC CORP
Author (Inventor): SHINOHARA HIROSHI; KISHI YOSHIYUKI
Priority (No,Kind,Date): JP 89213643 A 890819
Applic (No,Kind,Date): JP 89213643 A 890819
IPC: * H01L-021/3205
Derwent WPI Acc No: ; G 91-138287
JAPIO Reference No: ; 150246E000051
Language of Document: Japanese

PTO 03-4753

CY=JA DATE=19910402 KIND=A
PN=03-077324

SEMICONDUCTOR INTEGRATED CIRCUIT
[Handoutai shuuseki kairo]

Hiroshi Shinohara, et al.

UNITED STATES PATENT AND TRADEMARK OFFICE
Washington, D.C. August 2003

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INVENTORS (72): SHINOHARA, HIROSHI; KISHI, YOSHIYUKI

APPLICANT (71): MITSUBISHI ELECTRIC CORPORATION

TITLE (54): SEMICONDUCTOR INTEGRATED CIRCUIT

FOREIGN TITLE (54A): HANDOUTAI SHUUSEKI KAIRO

SPECIFICATION

1. Title of the Invention

Semiconductor Integrated Circuit

2. Claims

(1) A semiconductor integrated circuit that has multiple metal wiring layers and multiple wiring paths characterized by being equipped with a multilayer metal wiring means whereby multiple layers are overlapped in parallel on the same wiring path and are mutually connected via through-holes.

(2) In regard to a semiconductor integrated circuit equipped with cells that contain active devices and that occupy the cell regions on the semiconductor surface, equipped with pads that electrically connect to the exterior of the semiconductor integrated circuit, and equipped with outside-cell wiring regions that are outside the regions occupied by said cells or pads and that contain metal wirings for electrically connecting between the cells and between the cells and pads

a semiconductor integrated circuit of Claim 1 characterized by: having wide-range wirings that extend from cell regions to outside-cell wiring regions; these wide-range wirings being wired by means of said multilayer metal wiring means in at least one portion inside the cell regions and being wired by means of only 1 metal layer in at least one portion inside the outside-cell wiring regions; and the widths of said multilayer metal wiring means portions being narrower than the widths of said 1 metal layer portions.

3. Detailed Explanation of the Invention

[Field of Industrial Application]

The present invention pertains to wiring layout patterns for semiconductor integrated circuits.

[Prior Art]

For the wiring of a semiconductor integrated circuit, the loss of electrical power is reduced by using metal that has a small resistance value, such as Aℓ, an alloy of Aℓ, Si, and Cu, or W. Figure 7 is a partial plan view of a conventional semiconductor integrated circuit (inverter circuit). In the figure, [1] is metal wiring, [1a] is a power line, [1b] is a signal line, and [1c] is a grounding wire. [2] is a P^+ diffusion region, [3] is a n^+ diffusion region, [4] is polysilicon, [5] is a contact hole that connects the diffusion regions, [2] and [3], and the metal wiring, [1a], [1b], and [1c].

Next, the operation will be explained. The metal, such as Aℓ or an Aℓ alloy, utilized for the metal wiring [1] has a low melting point compared to the silicon compound that makes up a logic gate, and a phenomenon called electromigration, such as broken wiring or migration, occurs at high temperatures F or at current densities lower than $10^6 A/cm^2$.

In conventional metal wiring [1], the metal wiring [1] was made capable of withstanding a large current density by providing a sufficient wiring width in order to increase the strength against migration. In particular, the wiring width of signal wires having a large load capacity, such as the internal clock wire of the signal wire [1b], the power wire [1a], and the grounding wire [1c], is made to be wide so that the current

density becomes 10^6A/cm^2 or lower.

[Problems that the Invention is to Solve]

Since a conventional semiconductor integrated circuit's metal wiring is structured in the above manner, there is a problem in that the layout pattern (mask pattern) of the semiconductor circuit becomes large when the width is made sufficiently wide to withstand migration.

The present invention was completed in order to solve the above problem, and its purpose is to increase the strength against electromigration, to reduce the wiring region, and to obtain high integration as a result.

[Means for Solving the Problems]

The semiconductor integrated circuit pertaining to the present invention has multiple metal wiring layers and multiple wiring lines, and the metal wirings are connected to each other via through-holes by being overlapped in parallel on the same wiring line through the multiple layers.

[Operation of the Invention]

The metal wirings of the present invention are mutually connected via through-holes by the multiple layers being overlapped in parallel on the same wiring line. Therefore, the electric current can be divided, and the wiring widths can be narrowed while increasing the strength against electromigration, as well. This makes it possible to make the width of the metal wiring narrow and, as a result, to increase the integration of the semiconductor integrated circuit.

[Working Examples]

In the following, one working example of the semiconductor integrated circuit pertaining to the present invention will be explained based on drawings. Figure 1 is a plan view of the inverter circuit of the semiconductor integrated circuit that is one working example of the present invention, and Fig. 2 is a perspective drawing that is Fig. 1 viewed from [II]-[II] near the grounding wires. In addition, since [2]~[5] in the drawings are the same as those of said conventional one, their explanations will be omitted.

In the drawings, [7a] is a first-layer power wire formed with Aℓ metal wiring, [8a] is a second-layer power wire, [7b] is a first-layer signal wire, [8b] is a second-layer signal wire, [7c] is a first-layer grounding wire, [8c] is a second-layer grounding wire, and [6] is a through-hole. Moreover, an example in which the metal wiring is made from Aℓ is indicated in Figs. 1 and 2, but metal wiring for which an alloy of Aℓ and Si, of Aℓ and Si and Cu, or of Aℓ and Cu is utilized may be utilized instead of Aℓ.

Unlike the above-mentioned conventional article, the Aℓ metal wirings, such as the power wires, [7a] and [8a], signal wires, [7b] and [8b], grounding wires, [7c] and [8c], etc., are mutually connected via through-holes [6] by being overlapped in parallel on the same wiring line through two layers inside a semiconductor integrated circuit substrate that has multiple metal wiring layers and multiple wiring lines. Moreover, the widths of the Aℓ metal wirings, [7a], [7b], [7c], [8a], [8b], and [8c], are narrower than those of the conventional metal wirings, [1a],

[1b], and [1c]. Moreover, 1 through-hole [6] is utilized for Figs. 1 and 2, but it is permissible to use 2 or more instead. When the branching of the Aℓ metal wiring paths is taken into consideration, it is effective to provide the through-holes [6] at intervals, [ℓ], that are the widths of the metal wirings. One such example is shown in Fig. 3.

Next, the operation of the semiconductor integrated circuit will be explained. In the conventional wiring method, the metal wiring widths are made to be wide in order to keep the current density at $10^6 A/cm^2$ or below. For this reason, the ratio of the area occupied by the metal wiring widths becomes high in the semiconductor integrated circuit, and the total area of the semiconductor integrated circuit becomes large as a result.

In the present working example, instead of widening the metal wirings, the current is divided by using multiple layers and therefore, the current density can be kept low.

Figures 1 and 2 show an example in which two layers of metal wirings, which are [7a]-[8a], [7b]-[8b], and [7c]-[8c], are utilized, but 3 layers or more may be utilized instead. Moreover, because of the narrow wiring widths, the area of the semiconductor integrated circuit is smaller than that of a conventional one. Although a case in which multiple layers of metal wirings are overlapped was explained in the above working example, the same effects as those of the above working example are exhibited when the invention is applied to signal wires having large load capacities, such as power wires, grounding wires, clock wires, etc.

Next, another working example will be explained. There is a so-called cell-based design method in which a semiconductor integrated circuit is

built from the basic functional modules (cells) in a hierarchical manner when designing the semiconductor integrated circuit. Depending on the semiconductor integrated circuit designer, 1 transistor, 1 inverter circuit, etc., is considered one basic unit of a cell. A plan view of a semiconductor integrated circuit designed by the cell-based design method is shown in Fig. 4. This semiconductor integrated circuit is equipped with cells [9] which are functional modules containing active devices such as transistors, pads [10] that electrically connect with the exterior of the semiconductor integrated circuit, and outside-cell wiring regions [11] that contain metal wirings that electrically connect between the cells and between the cells and pads. As shown in the drawing, the shapes of the cells are often triangular in general, but they may be polygons (hexagons and octagons in the drawing) instead. For the design, cells [9] that are required for the semiconductor integrated circuit are positioned.

Any number of cells can be positioned depending on what is necessary. Figure 4 shows an example in which 7 cells [9] are positioned, but the functions of the cells may be either the same or different. After positioning the cells [9], metal wirings (wide-range wirings) (14) that electrically connect cells [9] to cells [9] and cells [9] to pads [10] are provided to the outside-cell wiring regions [11]. Wide-range wirings [14] cross over the inside-cell wiring regions [12] and outside-cell wiring regions [11], but at least a portion of the outside-cell wiring regions [11] is wired by means of only 1 metal layer. This is because the wirings [14] in the outside-cell wiring regions [11] are provided by using an

automatic wiring program, and at this time, the multiple layers of metal wirings are distinguished from each other by wiring the second-layer metal wirings in the direction perpendicular to that of the first-layer metal wirings.

In the past, wide-range wirings [14] that cross over the inside and outside of the cells had the same widths inside and outside of the cells. By using cells in which the metal wiring means of Figs. 1 ~ 3 are applied, the areas of the cells are reduced. As a result, the area of the semiconductor integrated circuit becomes smaller than that of a conventional case in which metal wirings are utilized. In particular, the wide-range wirings, which are 1 metal layers near the boundary of the inside-cell wiring region [12] and outside-cell wiring region [11] in this working example, are shown in Fig. 5. In Fig. 5, the metal wirings, [7] and [8], inside the cells are overlapped in parallel on the same wiring path through multiple layers and are mutually connected by means of through-holes [6]. The wide-range wiring in the outside-cell wiring region [11] has the conventional wiring width, but the wiring width inside the cell is narrow. Inside the area of the cell that is near the boundary between the inside and outside of the cell, a shape that is for shifting from the outside-cell wiring width (conventional wiring width) to the inside-cell multilayer metal wiring width is formed. Some other working examples are shown in Fig. 6. Figure 6 also shows examples in which 1 or 2 through-holes [6] are used, but any number of them may be provided.

[Effects of the Invention]

In the above manner, according to the present invention, it becomes possible to narrow the metal wiring widths of a semiconductor integrated circuit, and the area of the semiconductor integrated circuit becomes small. Also, even in a case in which a multilayer metal wiring means is utilized inside the cells, the areas of those cells become small, and as a result, many cells can be packaged in a semiconductor integrated circuit. Therefore, this leads to high integration of the circuit. Moreover, since the metal wirings are overlapped in parallel on the same wiring path through multiple layers and are connected via through-holes, the wirings become resistant against electromigration.

4. Brief Description of the Drawings

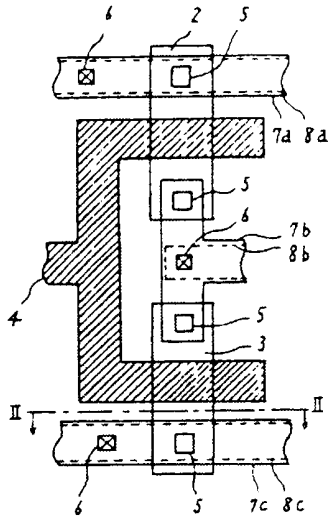
Figure 1 is a plane view of an inverter circuit that is one working example of the semiconductor integrated circuit pertaining to the present invention. Figure 2 is a perspective drawing obtained by viewing from the [II]-[II] line of Fig. 1. Figure 3 is a plane view that shows an example of the intervals between the through-holes of the multilayer metal wirings pertaining to the present invention, and the through-holes [6] are provided at intervals that are the same as the metal wiring widths. Figure 4 is a plane view of the semiconductor integrated circuit that is another working example of the present invention designed using a cell-based design method. Figure 5 is a magnified explanatory drawing showing metal wiring near the boundary between the inside and outside of the cell pertaining to the present invention. Figure 6 (a)~(h) are partial plan views showing other working examples of the metal wiring near the boundaries between

the inside and outside of the cells. Figure 7 is a plane view showing a conventional semiconductor integrated circuit.

In the drawings, [6] is a through-hole, [7] is the first-layer metal wiring of a case in which 2 layers of metal wirings are overlapped, [8] is a second-layer metal wiring, and [9] is a cell.

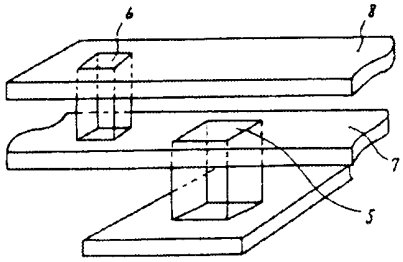
In addition, the same reference numerals inside the drawings indicate the same or equivalent parts.

Figure 1



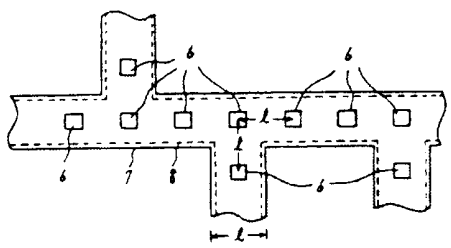
Key: 2) p^+ diffusion region; 3) n^+ diffusion region; 4) polysilicon; 5) contact hole; 7a) first-layer power wire; 8a) second-layer power wire; 7b) first-layer signal wire; 8b) second-layer signal wire; 7c) first-layer grounding wire; 8c) second-layer grounding wire.

Figure 2



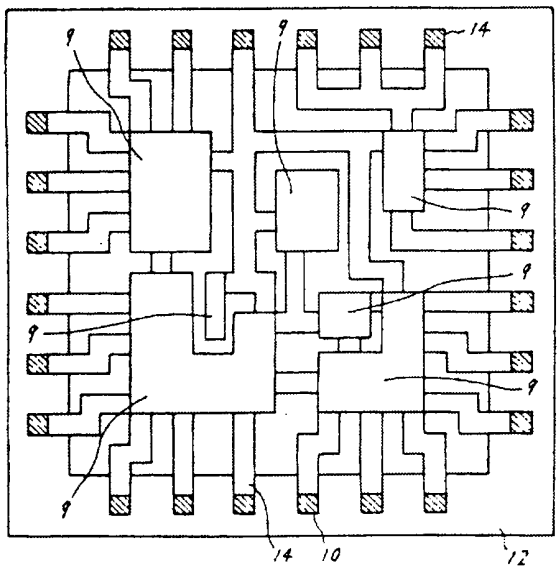
Key: 6) through-hole; 7) first-layer metal wiring (grounding wire); 8) second-layer metal wiring (grounding wire).

Figure 3



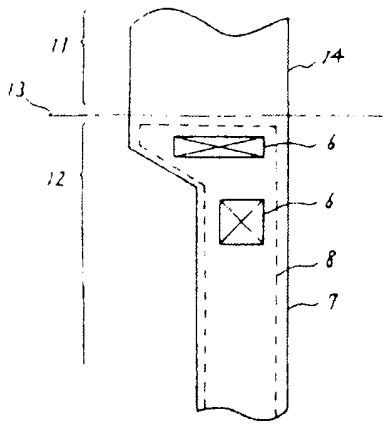
Key: 6) through-hole; 7) first-layer metal wiring; 8) second-layer metal wiring.

Figure 4



Key: 9) cell; 10) pad; 12) circuit substrate; 14) wide-range wiring.

Figure 5



Key: 6) through-hole; 7) first-layer metal wiring; 8) second-layer metal wiring; 11) outside-cell wiring region; 12) inside-cell wiring region; 13) boundary between the inside and outside the cell; 14) wide-range wiring.

Figure 6

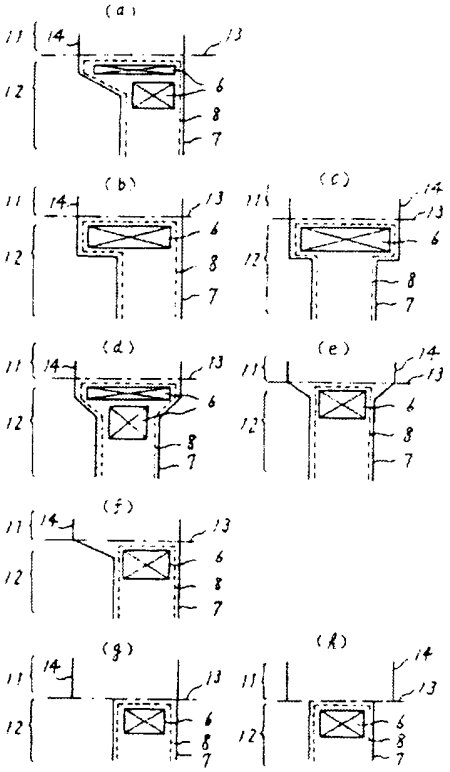
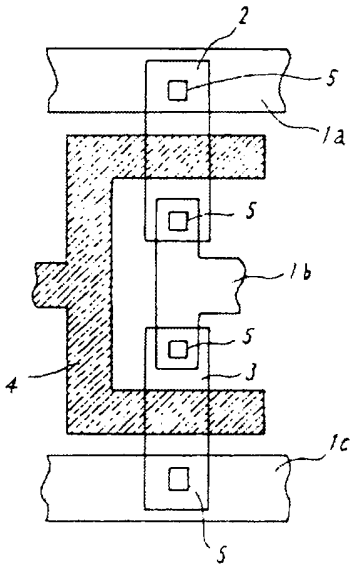


Figure 7



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⑤4発明の名称　半導体集積回路

⑳特　願　平1−213643
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明　細　書

1．発明の名称

半導体集積回路

2．特許請求の範囲

(1) 複数の金属配線層と複数の配線経路を有する半導体集積回路において、複数層にわたって同じ配線経路上を平行に重ね合わせ、スルーホールを介して互いに接続した多層金属配線手段を備えたことを特徴とする半導体集積回路。

(2) 能動素子を含み、半導体表面上のセル領域を占めるセルを備え、半導体集積回路外部との電気的接続を行うパッドを備え、前記セル及びパッドの占める領域外にあって、セル間及びセル−パッド間を電気的に接続する金属配線を含むセル外配線領域を備えた半導体集積回路において、

セル領域とセル外配線領域にわたる広域配線を有し、この広域配線はセル領域内の少なくとも一部分では前記多層金属配線手段で配線され、セル外配線領域内の少なくとも一部分では1層金属だけで配線され、前記多層金属配線手段部分の幅の方が、前記1層金属部分の幅よりも狭いことを特徴とする請求項1記載の半導体集積回路。

3．発明の詳細な説明

［産業上の利用分野］

本発明は半導体集積回路の配線レイアウトパターンに関するものである。

［従来の技術］

半導体集積回路における配線にはAlやAlとSi，Cuの合金，wなどの抵抗値の小さい金属を用いることにより電力の損失を少なくしている。第7図は従来の半導体集積回路（インバータ回路）の部分平面図である。図において、(1)は金属配線で、(1a)は電源線、(1b)は信号線、(1c)は接地線である。(2)はP⁺拡散領域、(4)はn⁺拡散領域、(4)はポリシリコン、(5)は拡散領域(2)，(3)と金属配線(1a)，(1b)，(1c)を接続するコンタクトホール(5)である。

次に動作について説明する。金属配線(1)に用いられるAl,Al合金等の金属は論理ゲートを構成するシリコン化合物に比べて融点が低く、高温下や$10^6A/cm^2$の電流密度下ではエレクトロ・マイグレーションといわれる断線や移動といった現象が起こる。

従来の金属配線(1)ではマイグレーションに対する強化策として、充分な配線幅を設けることによって大電流密度に耐える金属配線(1)にしていた。特に電源線(1a)、接地線(1c)および信号線(1b)の内クロック線等の負荷容量の大きい信号線の配線幅は広く設けて、電流密度が$10^6A/cm^2$以下になるようにされていた。

[発明が解決しようとする課題]

従来の半導体集積回路の金属配線は以上のように構成されていたので、マイグレーションに耐えうるに充分な幅を設けることにより半導体集積回路のレイアウト・パターン(マスクパターン)が大きくなるという問題点があった。

本発明は上記のような問題点を解決するためになされたもので、エレクトロマイグレーションに強く、かつ配線領域を小さくし、結果として高集積化を得ることを目的とする。

[課題を解決するための手段]

本発明に係る半導体集積回路は複数の金属配線層と複数の配線線路を有し、金属配線を複数層にわたって同じ配線線路上平行に重ね合わせ、スルーホールを介して互いに接続するようにしたものである。

[作用]

本発明における金属配線は複数層にわたって同じ配線線路上平行に重ね合わせスルーホールを介して互いに接続されているので、電流を分配することができるとともに配線幅はエレクトロマイグレーションについて強化しながら狭くすることが可能となり、金属配線幅が狭くでき結果として半導体集積回路の高集積化を計ることができる。

[実施例]

以下、本発明に係る半導体集積回路の一実施例を図について説明する。第1図は本発明の一実施例である半導体集積回路のインバータ回路の平面図、第2図は第1図における接地線付近II-IIから見た斜視図を示している。なお、図中符号(2)～(5)は前記従来のものと同一につき説明は省略する。

図において、(7a)はAl金属配線で形成された第1層電源線、(8a)は第2層電源線、(7b)第1層信号線、(8b)は第2層信号線、(7c)は第1層接地線、(8c)は第2層接地線、(6)はスルーホールである。なお、第1図および第2図ではAlによる金属配線の例を示したがAl以外にもAlとSi,Alとの合金を用いた金属配線でもよい。

前記従来のものとは異なり、第1図および第2図では電源線(7a),(8a)信号線(7b),(8b)、接地線(7c),(8c)等のAl金属配線は複数の金属配線層と複数の配線線路を有する半導体集積回路基板中、2層にわたって同一配線線路上平行に重ね合わせ、スルーホール(6)を介して互いに接続されている。又、Al金属配線(7a),(7b),(7c),(8a),(8b),(8c)の幅は従来の金属配線(1a),(1b),(1c)に比べて狭い。また、第1図および第2図ではスルーホール(6)は1つずつ用いているが2個以上でもよい。Al金属配線経路が枝別れすることを考慮すると、スルーホール(5)は金属配線幅の間隔1で設けるのが有効である。その一例を第3図に示す。

次に半導体集積回路の動作について説明する。従来の配線方法では電流密度を$10^6A/cm^2$以下に抑えるために金属配線幅を広くしていた。そのため半導体集積回路において金属配線幅の占める面積の割合が大きくなり、結果として半導体集積回路全体の面積は大きくなる。

本実施例では金属配線の幅を広くするのではなく、複数層にすることによって電流を分配し、電流密度を抑えることができる。

第1図および第2図では(7a)-(8a),(7b)-(8b),(7c)-(8c)といった2層の金属配線層の例を示したが、3層以上でもよい。また配線幅が狭いことにより、半導体集積回路の面積は従来のものに比

へてゆくことになる。上記実施例では金属配線は全て両方向配線とした場合について説明したが、電源線、接地線、クロック線等の信頼性重の大きい信号線を用いた場合も上記実施例と同様の効果がある。

次に他の実施例について説明する。半導体集積回路を設計する際に、半導体集積回路を基本機能セル（セル）から階層的に構築していく、いわゆるセルベース設計方式がある。セルは半導体集積回路設計者にとって、トランジスタ1個とかインバータ回路1個等を1つの基本単位として考えられる。セルベース設計方式によって設計された半導体集積回路の平面図を第4図に示す。この半導体集積回路はトランジスタ等の能動素子を含む機能ブロックであるセル(3)と半導体集積回路外部との電気的接続を行うパッド(10)と、セル間及びセル－パッド間を電気的に接続する金属配線を含むセル外配線領域(11)を備えている。図に示すようにセルの形は一般には4角形が多いが、多角形（図では6角形、8角形）でもよい。

設計には半導体集積回路に要求されるセル(3)を配置する。

配置するセル数は必要に応じて何個でもよい。又、第4図ではセル(3)を7個配置した場合を示したが、各々のセルの機能は同じであっても異なっていてもよい。セル(3)を配置した後、セル外配線領域(11)に、セル(3)とセル(9)、セル(9)とパッド(10)を電気的に接続する金属配線（広域配線）(14)がなされる。広域配線(14)はセル内配線領域(12)とセル外配線領域(11)にまたがっているが、セル外配線領域(11)の少なくとも一部分では1層金属だけで配線されている。その理由はセル外配線領域(11)における配線(14)は自動配線プログラムを用いてなされ、その時、複数層にわたる金属配線は第1層金属配線に対して第2層金属配線は垂直方向に配線するといった具合に層を区別して用いるからである。

従来、セル内外にまたがる広域配線(14)はセル内、セル外ともに同じ配線幅であったが、セル内においては第1図～第3図の金属配線手段を適用したセルを用いることでセルの面積は小さくなり、その結果、半導体集積回路の面積は従来のものによる金属配線を用いた場合よりも小さくなる。特にこの実施例においてセル内配線領域(12)とセル外配線領域(11)の境界近傍において1層金属になっている広域配線について第5図に示す。第5図においてセル内の金属配線(7),(8)は複数層にわたって同じ配線経路上平行に重ね合わせられ、スルーホール(6)によって互いに接続されている。セル外配線領域(11)における広域配線は従来の配線幅であるが、セル内においては配線幅が狭くなっている。セル内外の境界近傍のセル内においてはセル外配線の幅（従来の配線幅）からセル内の多層金属配線幅へ移行するための形が形成されている。そのいくつかの他の実施例を第6図に示す。第6図においてもスルーホール(6)を1つ又は2つ用いた例を示したが何個設けてもよい。

【発明の効果】

以上のように本発明によれば、半導体集積回路における金属配線幅を狭くすることが可能となり、半導体集積回路の面積は小さくなる。又、セル内において多層金属配線手段を適用した場合についてもそのセルの面積は小さくなり、その結果、半導体集積回路に多くのセルを組み込むことが出来るので、回路の高集積化につながる。又、金属配線は同じ配線経路上、複数層にわたって平行に重ね合わされてスルーホールによって接続されているので、エレクトロ・マイグレーションに強い配線となるなどの効果が得られる。

4．図面の簡単な説明

第1図は本発明に係る半導体集積回路の一実施例を示したインバータ回路の平面図、第2図は第1図のII－II線より見た斜視図、第3図は本発明に係る多層金属配線におけるスルーホールの開孔についての例を示した平面図で、スルーホール(6)は金属配線幅の開孔で設けている。第4図はセルベース設計方式により設計された本発明の他の実施例を示した半導体集積回路の平面図、第5図は本発明に係るセル内外の境界近傍の金属

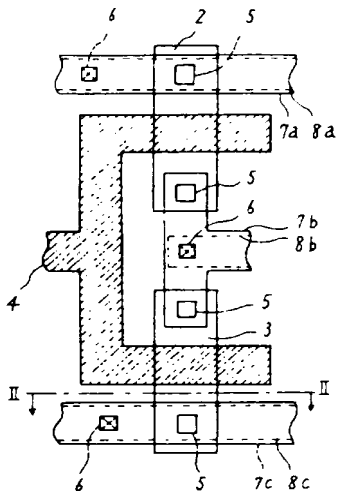
配線を示した拡大説明図、第６図(a)～(h)はセル内外の境界近傍の金属配線の他の実施例を示した部分平面図、第７図は従来の半導体集積回路を示した平面図である。

図において、(6)はスルーホール、(7)は２層の金属配線を重ねた時の第１層金属配線、(8)は第２層金属配線、(9)はセルである。

なお、図中、同一符号は同一、または相当部分を示す。

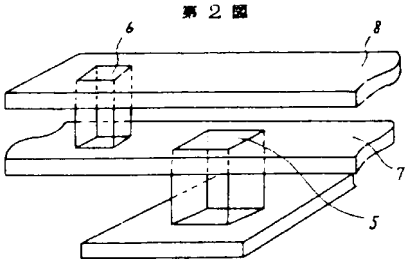
代理人　大　岩　増　雄

第１図



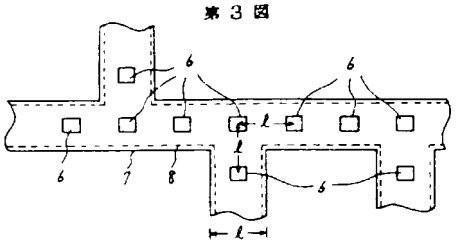
2 P⁺拡散領域　　7a 第1層電源線
3 N⁺拡散領域　　8a 第2層電源線
4 ポリシリコン　　7b 第1層信号線
5 コンタクトホール　　8b 第2層信号線
7c 第1層接地線
8c 第2層接地線

第２図



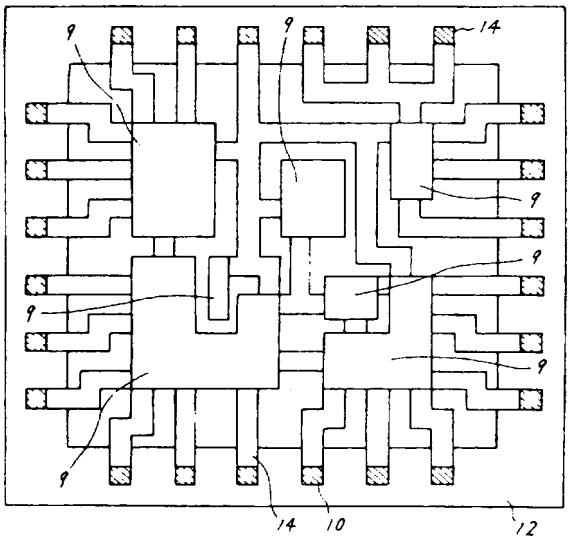
6 スルーホール
7 第1層金属配線（接地線）
8 第2層金属配線（接地線）

第３図



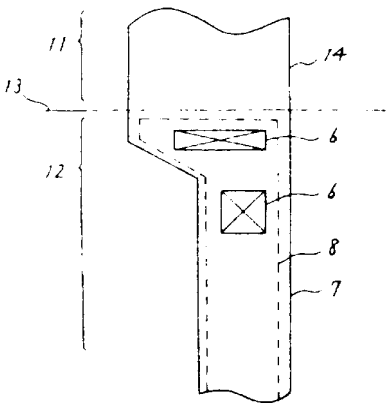
6 スルーホール
7 第1層金属配線
8 第2層金属配線

第４図



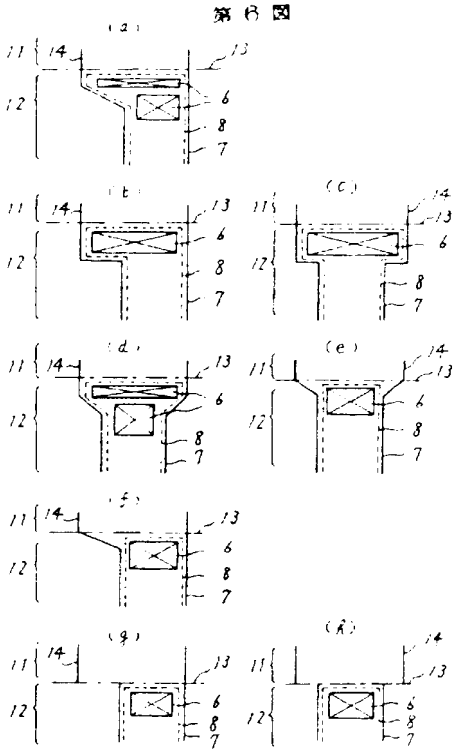
9 セル　　12 回路基板
10 パッド　　14 広域配線

第5図



6：スルーホール　12：セル内配線領域
7：第1層金属配線　13：セル内外境界
8：第2層金属配線　14：広域配線
11：セル外配線領域

第6図



第7図